HORIZONTAL MEMORY DEVICES WITH VERTICAL GATES

Cross Reference To Related Applications

This application is related to the following co-pending, commonly assigned U.S. patent applications: "Programmable Logic Arrays with Transistors with Vertical Gates," attorney docket no. 303.683US1, serial number 09/583,584, and "Programmable Memory Decode Circuits with Vertical Gates," attorney docket no. 303.692US1, serial number 09/584,564, which are filed on even date herewith and each of which disclosure is herein incorporated by reference.

Technical Field of the Invention

This invention relates generally to integrated circuits and in particular to horizontal memory devices with vertical gates.

Background of the Invention

One difficulty with EEPROM, EAPROM, and flash memory devices is the adverse capacitance ratio between the control gate and the floating gate. That is, the capacitance between the control gate to floating gate (CCG) is about the same as the floating gate to substrate capacitance (CFG). Figure 1A is an illustration of a horizontal EEPROM, EAPROM, or flash memory device formed according to the teachings of the prior art. As shown in Figure 1A, conventional horizontal floating gate transistor structures include a source region 110 and a drain region 112 separated by a channel region 106 in a horizontal substrate 100. A floating gate 104 is separated by a thin tunnel gate oxide 105 shown with a thickness (t1). A control gate 102 is separated from the floating gate 104 by an intergate dielectric 103 shown with a thickness (t2). Such conventional devices must by necessity have a control gate 102 and a floating gate 104 which are about the same size in width.